

WHAT IS CLAIMED IS

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1. A semiconductor memory device comprising:

an input circuit for receiving data to be written into a memory cell array and outputting the 10 received data to write buffer circuits that write the received data into the memory cell array;

an output circuit for outputting read data to the outside, each element of the read data having been read out from the memory cell array and 15 amplified by a corresponding sense amplifier;

an input controller for controlling the input circuit so that the input circuit receives the received data only during a predetermined period;

a plurality of input data lines for 20 transmitting the received data from the input circuit to the write buffer circuits; and

a plurality of output data lines for transmitting the data amplified by the sense amplifiers to the output circuit;

25 wherein the input data lines and the

output data lines are alternatingly and adjoiningingly disposed on the semiconductor memory device.

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2. The semiconductor memory device as claimed in claim 1, wherein the input controller controls the input circuit so that the input circuit 10 inputs the data to be written in synchronization with a leading edge of an external clock signal.

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3. The semiconductor memory device as claimed in claim 2, wherein the input controller generates an internal clock signal based on a predetermined external clock signal; and 20 the input controller controls the input circuit so that the input circuit inputs the data to be written after an external write enable signal becomes an enable state and during a predetermined period since the internal clock signal has become a 25 predetermined signal level.

5 4. The semiconductor memory device as
claimed in claim 1, further comprising a signal line
connected to a power supply or ground, the signal
line being disposed outside of the outermost output
data line.

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5. The semiconductor memory device as
15 claimed in claim 1, further comprising:
 a complimentary data generator for
generating and outputting complimentary data of the
data transmitted by each of the input data lines;
and
20 a plurality of input complementary data
lines for transmitting the complementary data from
the complimentary data generator to the write buffer
circuit;
 wherein each of the output data lines is
25 disposed between the corresponding input data line

and its corresponding input complementary data line.

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6. The semiconductor memory device as
claimed in claim 1, wherein the output data lines
transmit latched output signals from the sense
amplifiers, and the latched output signals are
10 shielded by the input data lines.

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7. The semiconductor memory device as
claimed in claim 1, wherein,
during a writing operation, the input
circuit outputs the received data to the input data
lines; and
20 during a reading operation, the output
circuit holds data inputted immediately before the
reading operation and outputs the inputted data to
the input data lines.

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8. The semiconductor memory device as
claimed in claim 1, further comprising:

5 a plurality of bypass circuits, each of
the bypass circuits being disposed between a
corresponding input data line and a corresponding
output data line, and transmitting the data on the
corresponding input data line to the corresponding
10 output data line.